innovation for industry

State of the art in silicon photonics and technology roadmap

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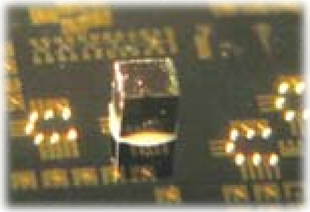
Why silicon ?

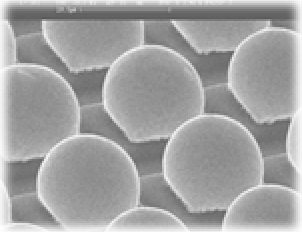
- Transparent in the near IR
- High index contrast = miniaturisation
- CMOS compatible
- Low cost

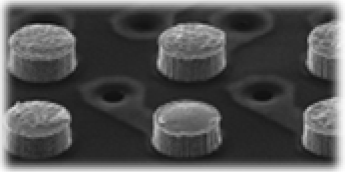
- No photodetection in 1.2µm to 1.6µm → Ge photodiodes
- High index contrast= coupling with fiber difficult → interfaces
- No electro-optic effect→Carrier depletion modulation
- No efficient light emission→ external source or III-V/Si heterogeneous integration

Photonic Electronic Integration

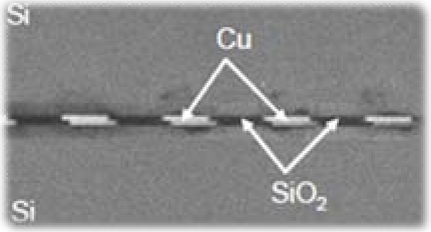


- Die to wafer integration
  - Stud bumping (low number of pins)
  - Flip-chip (high number of pins)
  - Cu pillars
  - *Higher yield*
  - *Adapted to chips of different size*

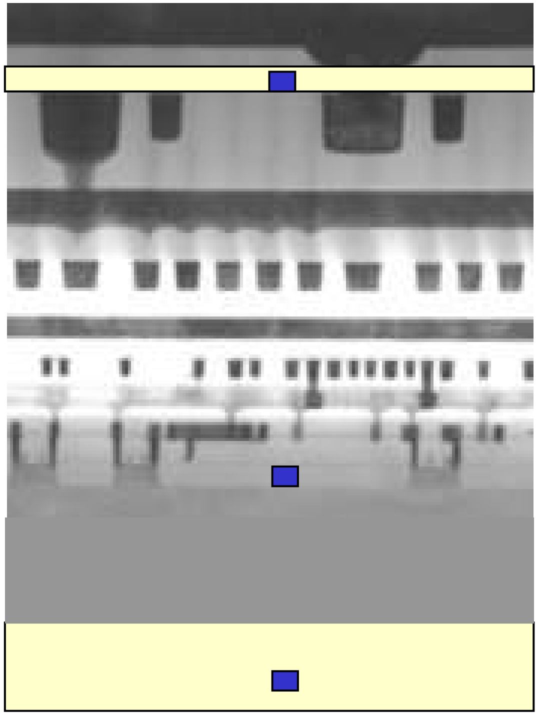




- Wafer scale integration
  - Front end or Back end
  - *Yield issues*
  - *Similar chip size required*



Wafer Integration of photonics on CMOS



Option 1
Photonic layer at the last levels of metallizations with back-end fabrication

- FE fab with wafer bonding (1A) or BE fab(1B)
- Use of standard FE CMOS technologies
- Heterogeneous integration of III-V on Si
- High integration density (AboveIC)
- Multilevel process capability

Option 2
Combined front-end fabrication

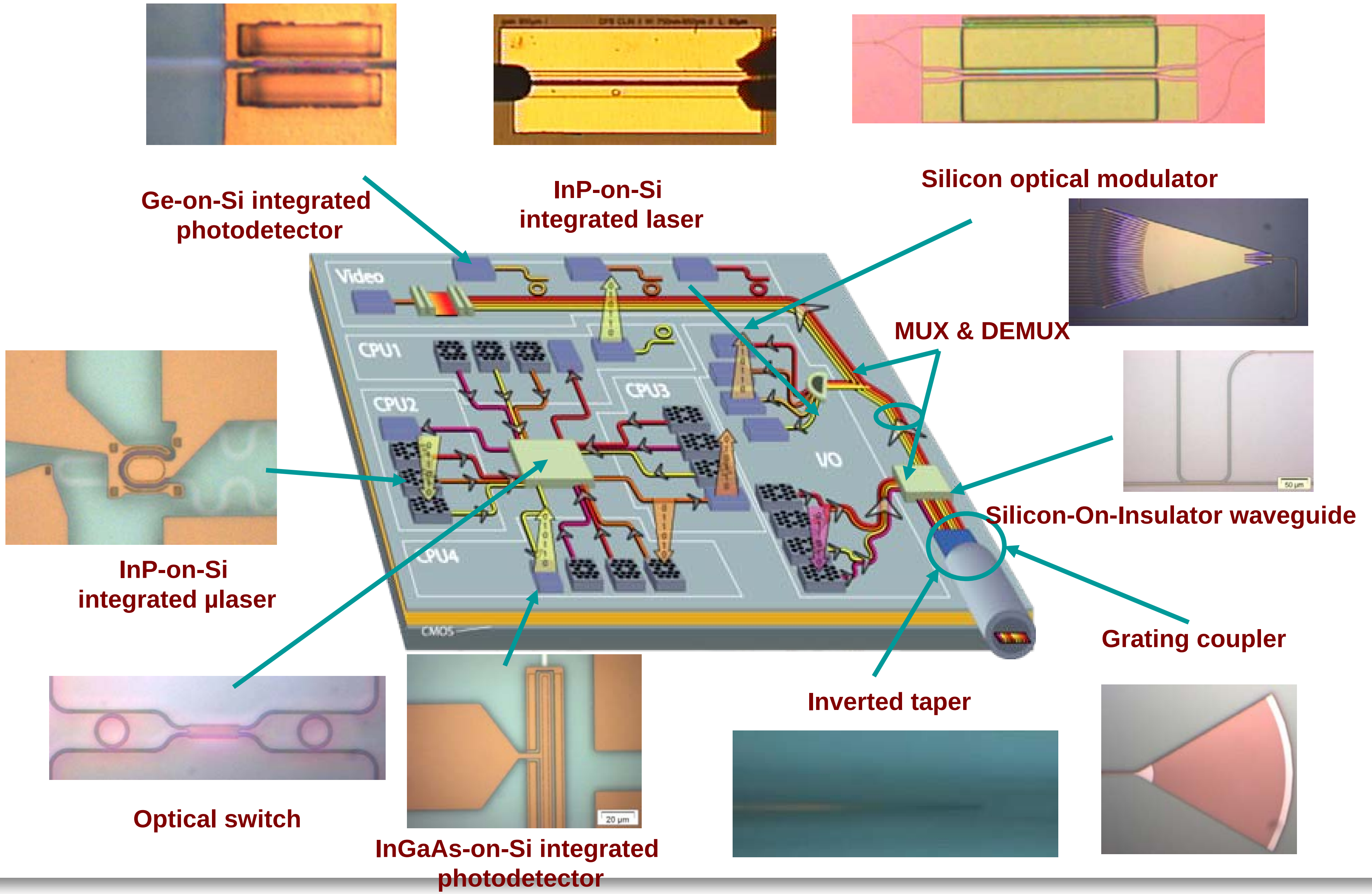
- Specific FE CMOS technology and library
- Flip-Chip hybridization of InP components
- Moderate integration density
- Efficient connections of EIC and PIC

Option 3
Backside fabrication

- BE fab(<400°C) or FE fab with wafer bonding
- Through substrate connections
- High integration density
- Heterogeneous integration of III-V on Si

BE: Back end FE:Front end

Main achievements



InP Laser on Si results

- Major players: INTEL,UCSB, LETI, UGent (IMEC)

Specifications sources	UCSB	LETI	INTEL	UCSB	UCSB
Type	Si DBR	Si DBR	Si DBR	Ring	Si DFB
Output power (mW) 20°C	11	14	30	29	5.4
Ith (mA)	65	40	45	175	25
SMSR (dB)	50	>20			50
T° max operation	45	60	90°C	60	50
	DML : ER 6 dB for data rates 4 GB/s	1550nm DML : data rates 5 GB/s	1300nm		

Modulation results

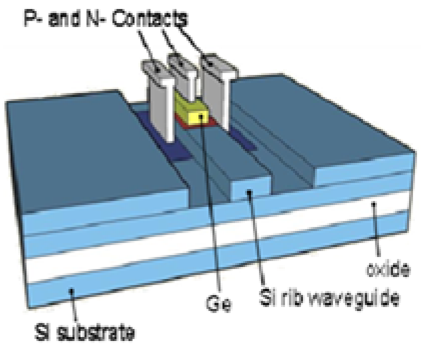
Specifications modulators	UNIS+LETI (Thin modulator)	IEF+LETI (Thick modulator)	Lightwire	INTEL	UNIS+LETI	UCSB
Modulation scheme :	Carrier Depletion in lateral pn Junction	Carrier Depletion in a doped slit in a lateral PIN diode	Carrier Accumulation	Carrier Depletion in a vertical pin diode	Carrier Depletion in a vertical pin diode	III-V Bonded electro absorption (500µm)
Structure	MZI	MZI	MZI	MZI	MZI	Waveguide
Insertion loss	7dB	5dB	-	7dB	7.7dB	1,5dB
3dB bandwidth	8GHz	15GHz	-	30GHz	?	25GHz
$V\pi L$	6V.cm	5V.cm	0.2V.cm	4V.cm	?	0,24V.cm
Extinction Ratio	7dB	8db	8.9 dB	1 dB	6.5dB	19.5db
Tx rate	10Gbit/s	10Gbit/s	10Gbit/s	40Gbit/s	40Gbit/s	40Gbit/s

Photodiodes results

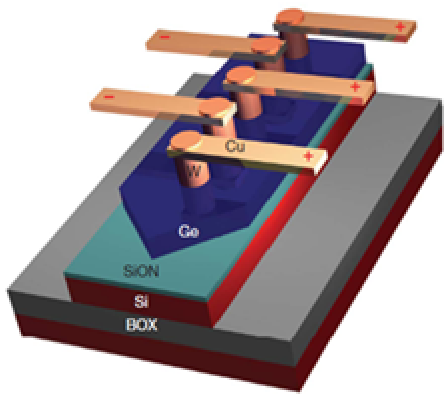
Specifications WP5 Photodetection	**IEF+LETI**	**IEF+LETI**	**UGhent**	**Intel**	**TUE**	**Luxtera**	**Intel**
Type	Ge PIN vertical	Ge PIN lateral	InGaAs	InGaAs	InGaAs	Ge PIN lateral	Ge PIN vertical
3 dB bandwidth	**42 GHz**	**130 GHz**	35GHz (th)	<10GHz	>20GHz	20GHz	31GHz
Responsivity (A/W)	1	0.8	1	1.2	0.45	0.85	0.9
Dark current	20 nA	2 µA	**5 nA**	50 nA	2 nA	10 µA	170 nA
Rx rate	**40Gbit/s @ -4V**	**10Gbit/s @ -0V**				10Gbit/s	40 Gbit/s @ -5V

Avalanche photodiodes

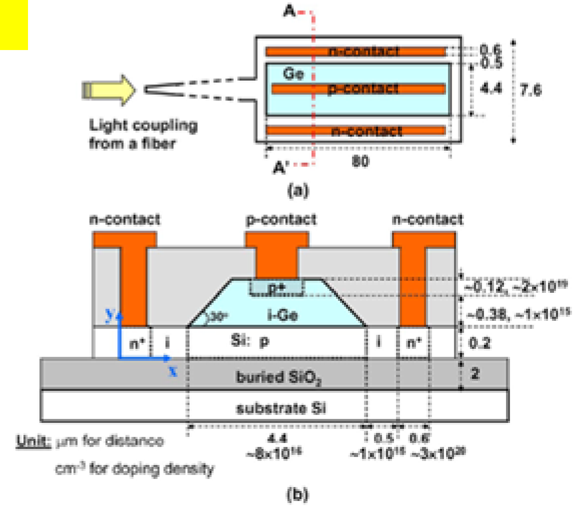
[1] Z. Huang et al., Group IV Photonics 2010 FA2 (2010)
[2] S Assefa et al. Nature 464, 80-84 (2010)
[3] S. Zhu et al., IEEE Electron Device Letters 30, 934 (2009)



(a)



(b)

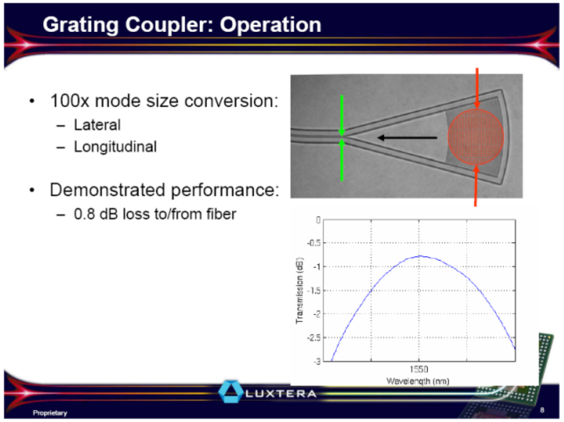


(c)

	Intel [1]	IBM[2]	A*Star[3]
Gain	10	10	26
BW	29.5 GHz	30 GHz	3.3 GHz
GBW	300 GHz	300 GHz	85 GHz
Reverse voltage	22V	1.5 V	22 V
F	-	3	4
Dark current	~20-30μA	50mA	22μA at - 22V

I/O couplers

- Diffractive structures
  - Basic (IMEC, UPS): up to 55%, 35nm 1dB bandwidth
  - Bottom mirror: (IMEC) 69%
  - Overlay (Luxtera, IMEC) > 85%
- Ideal for waferscale testing
- 2D-grating allows polarisation diversity



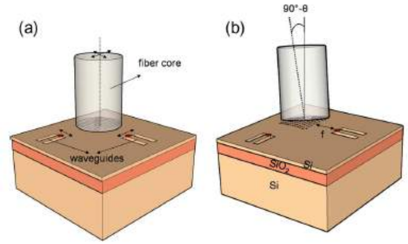


Fig. 1. (a) Vertical coupling. (b) Near-vertical coupling. In this case, the fiber is tilted along the bisection line of the grating.

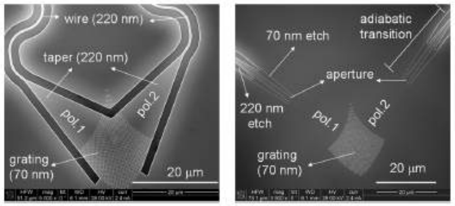
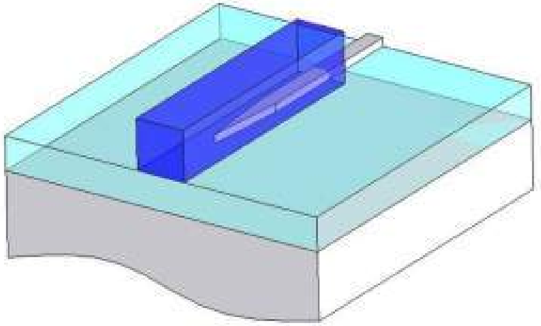


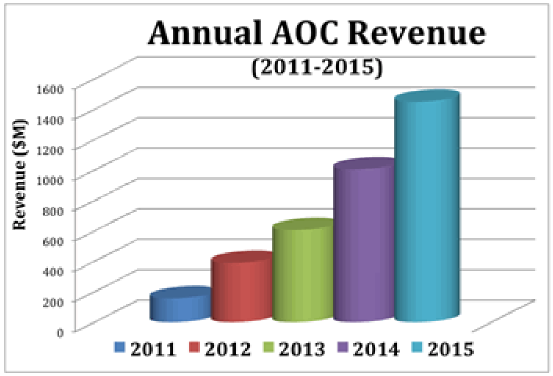
Fig. 3. SEM-pictures of focusing 2-D-grating couplers using a two-step etch process (70 and 220 nm depth). Left: short nonadiabatic taper configuration. Right: Shallow aperture configuration.

- Adiabatic structures
  - Demonstrated by NTT, MIT, IMEC, LETI, IBM
  - <2dB coupling loss
  - Wide bandwidth
  - Non ready compatible with waferscale testing
  - Compatible with standard edge-coupling approaches

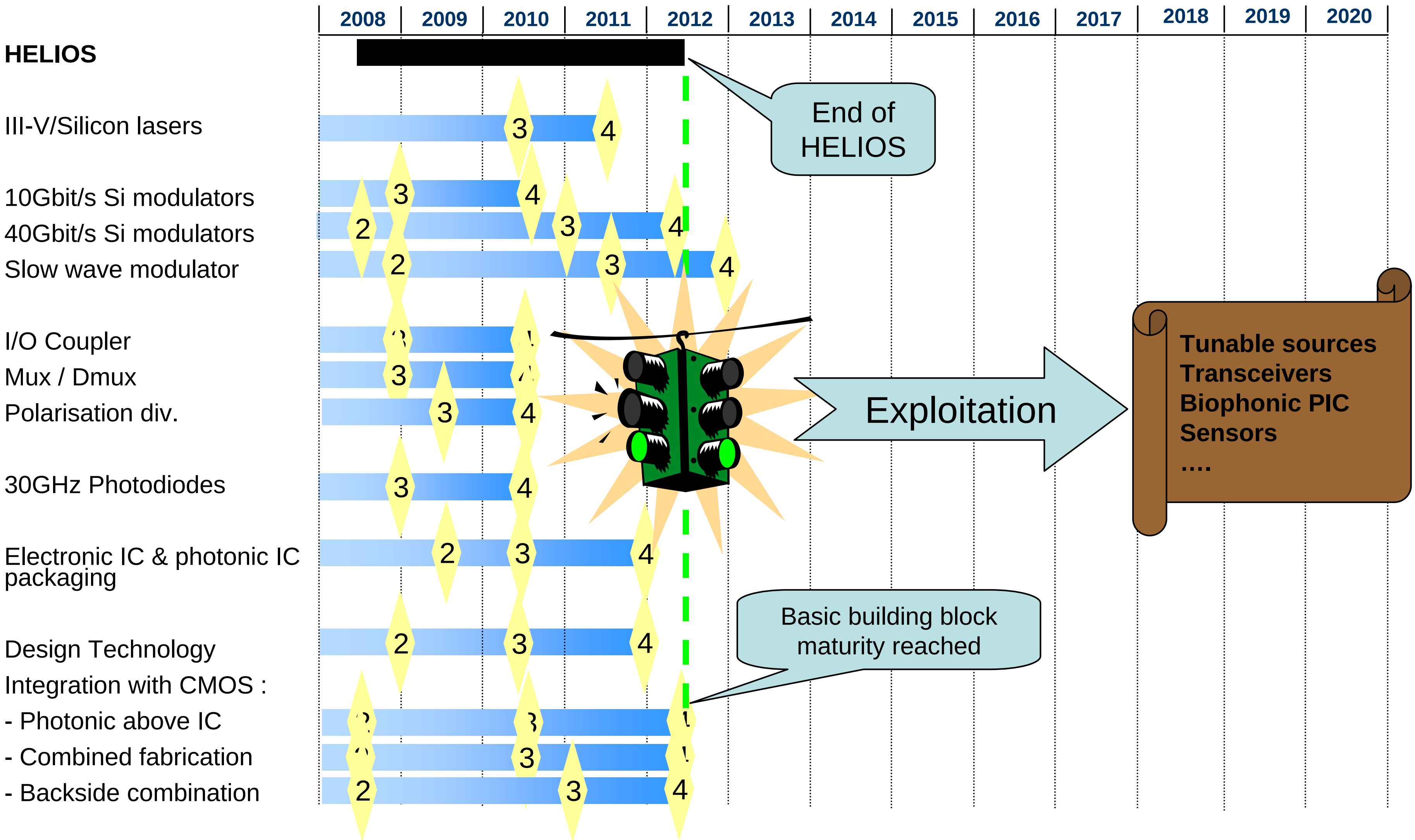


Focus on Datacoms

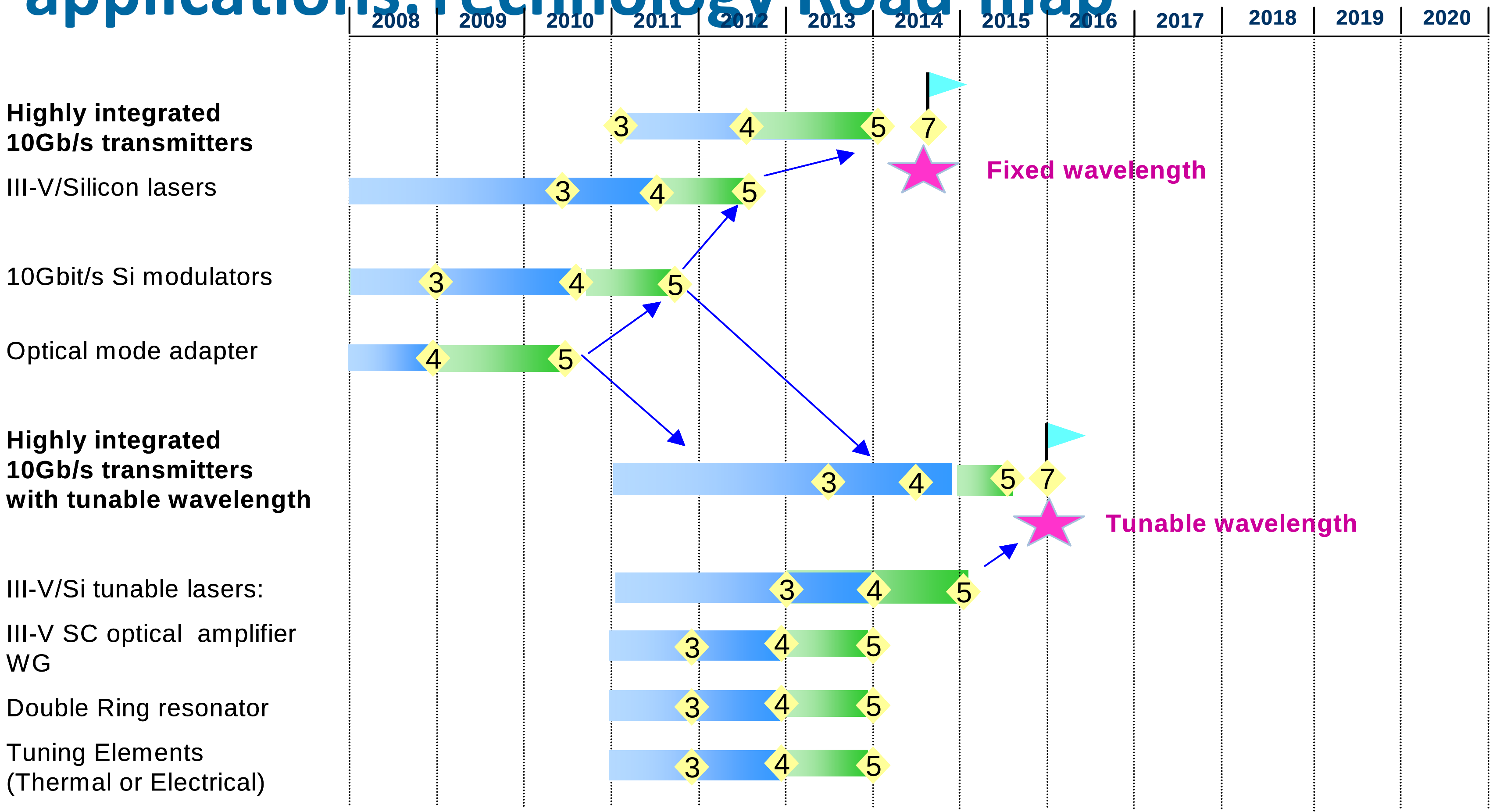
- Active Optical Cables: datacenters, HPC, servers
- Major trend: increase in channel bitrate:
  - Infiniband FDR (14Gb/s) and EDR (26Gb/s) starting in 2011
  - 100Gb Ethernet (4x25Gb/s)
  - 16GFC Fiber Channel @14Gb/s
- VCSELs based solutions are limited →oppportunity for silicon photonics
- First silicon photonics products



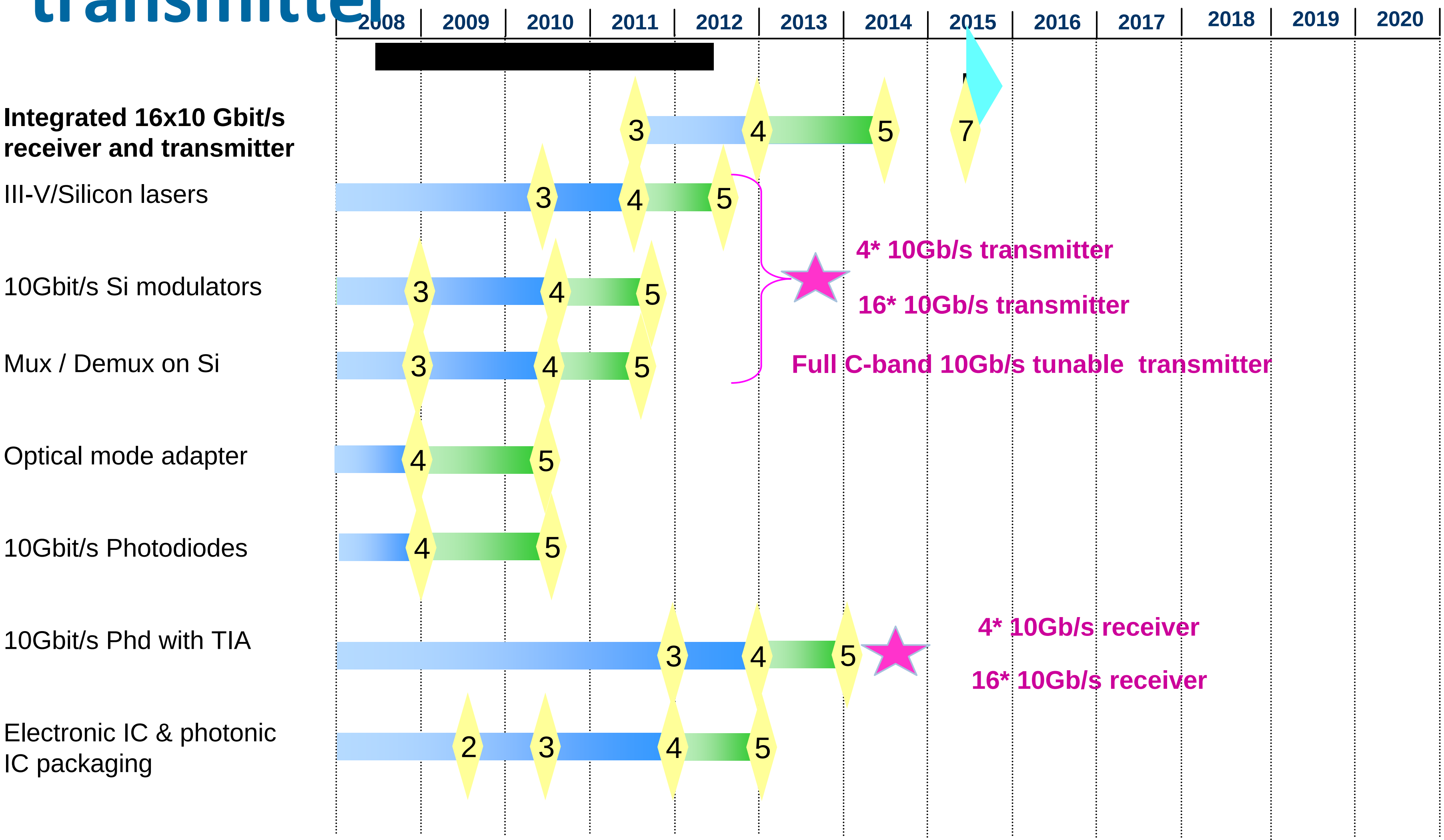
Helios Component Roadmap



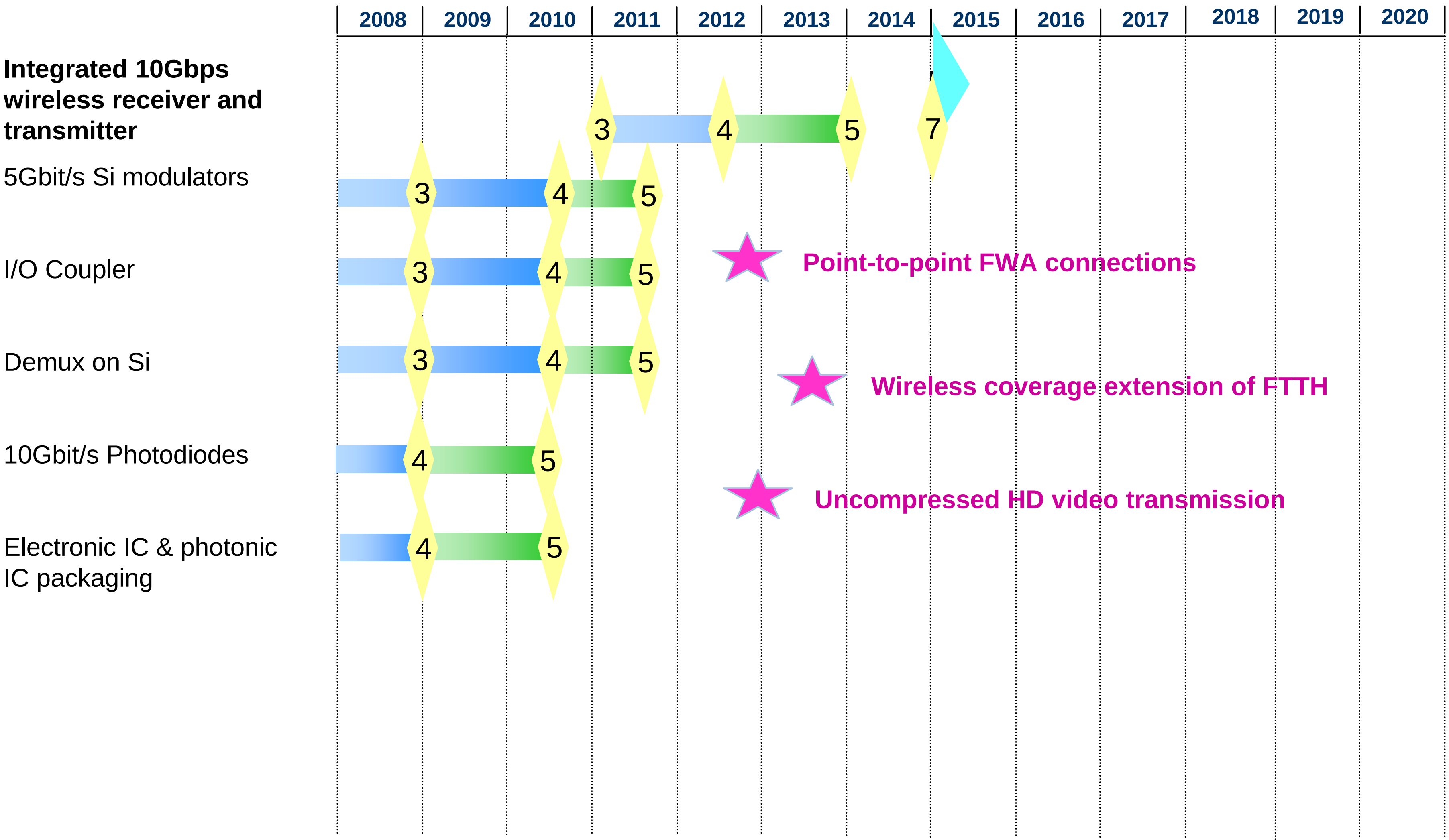
Tunable sources for metro/ access applications:Technology Road-map



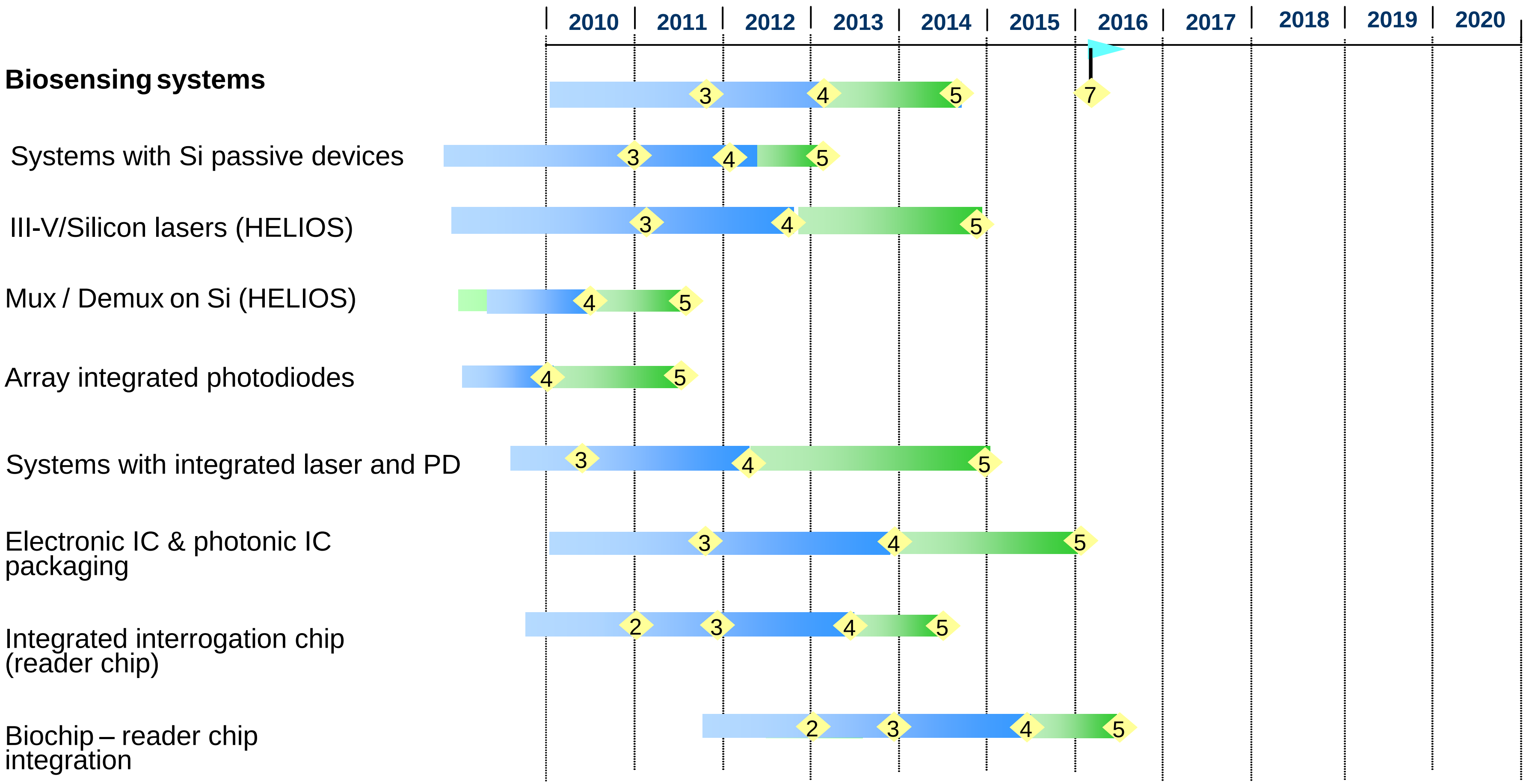
Integrated 16x10 Gbit/s receiver and transmitter



10Gbps wireless systems



Sensors & Biophotonics



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Thanks for your attention