

ePIXfab

Pieter Dumon



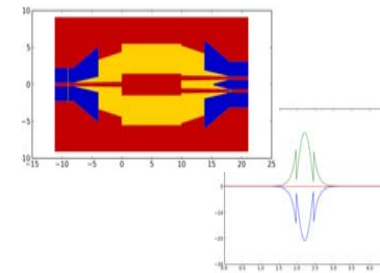
ePIXfab

Access to silicon photonics technology for academic and industry R&D

Outreach events MPW services Training



CAD



Transfer to production

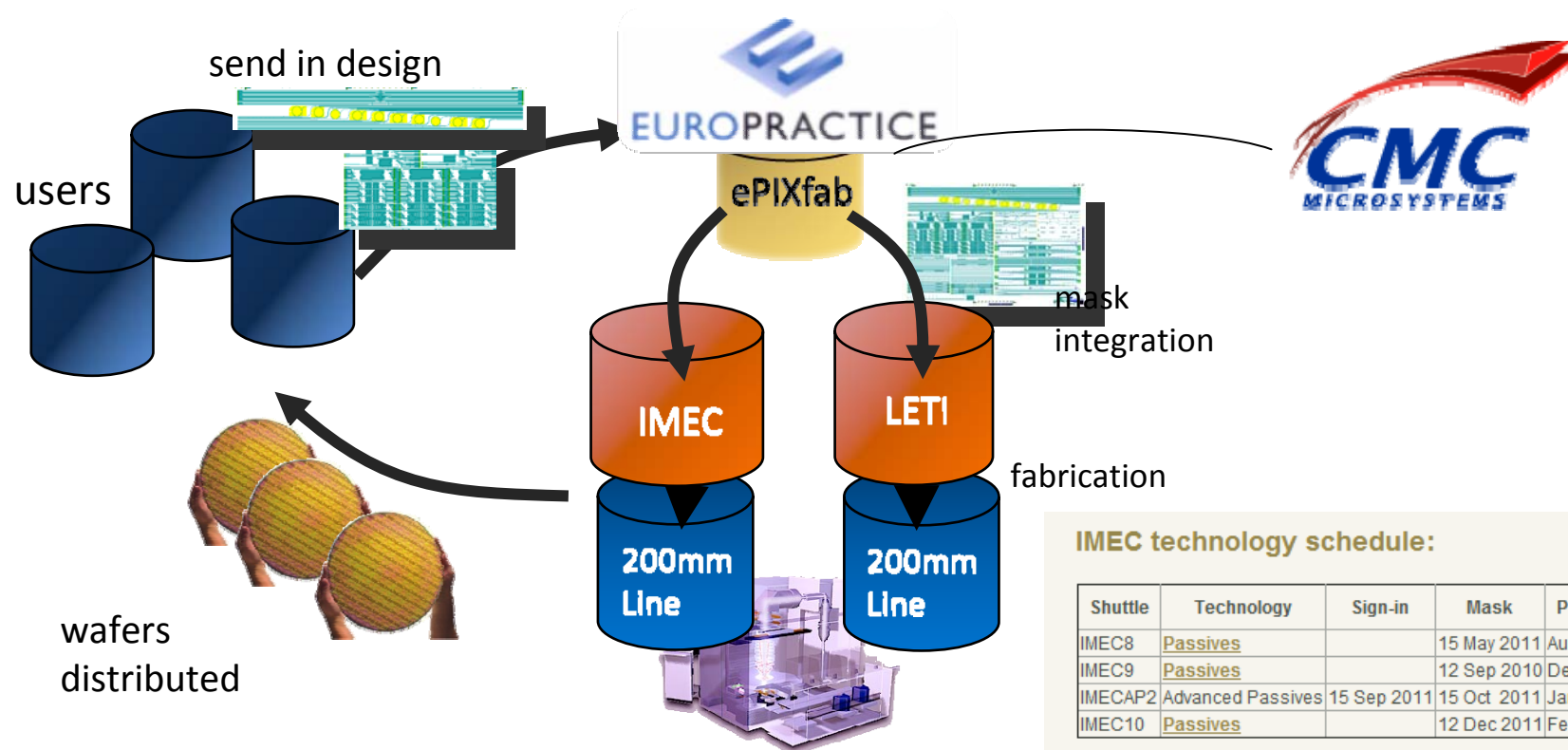


Partially funded by the EC



www.epixnet.org
www.photonfab.eu

MPW shuttle service



IMEC technology schedule:

Shuttle	Technology	Sign-in	Mask	Processed	Broker
IMEC8	Passives		15 May 2011	Aug 2011	Europractice
IMEC9	Passives		12 Sep 2010	Dec 2011	Europractice
IMECAP2	Advanced Passives	15 Sep 2011	15 Oct 2011	Jan 2012	ePIXfab
IMEC10	Passives		12 Dec 2011	Feb 2012	Europractice

LETI technology schedule:

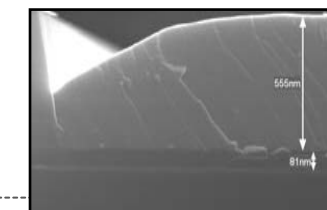
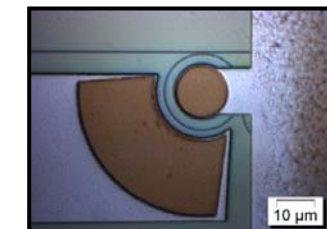
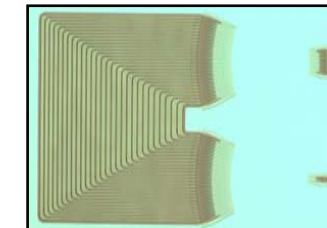
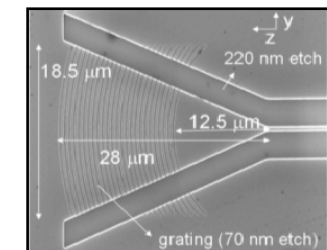
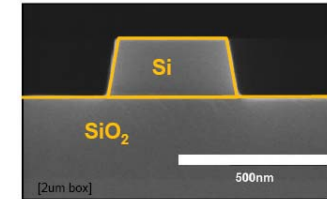
Shuttle	Technology	Sign-in	Mask	Processed	Broker
LETI6	STD	31 Jan 2011	28 Feb 2011	May 2011	ePIXfab
LETI6	FLEX	31 Jan 2011	28 Feb 2011	process flow dependant	ePIXfab
LETI7	STD	30 Jun 2011	31 July 2011	Oct 2011	Europractice
LETI7	FLEX	30 Jun 2011	31 July 2011	process flow dependant	ePIXfab

MPW service

- Technologies:
 - Imec
 - LETI
- CAD software:
 - PhoeniX
 - Ugent-Imec
 - Design Workshop
 - Mentor Graphics

Technologies

- **Imec:**
 - 2-layer and 4-layer passive device processes
 - Edge couplers (Ugent)
 - 2012: modulators & heaters
 - 200mm wafer fab, ~0.13um technology, industrial tooling
- **CEA-LETI:**
 - 2 layer passive device process
 - Thermo-optic heaters
 - 200mm wafer fab, ~0.13um technology , industrial tooling
 - + Flexible access to implants, contacts, Ge epitaxy, metalization



Europractice IC



EUROPRACTICE

www.europractice-ic.com

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EUROPRACTICE IC Service

The EUROPRACTICE IC Service brings ASIC design and manufacturing capability within the technical and financial reach of any company that wishes to use ASICs.

The EUROPRACTICE IC Service, offered by IMEC and Fraunhofer, offers low-cost ASIC prototyping and ASIC small volume production ramp-up to high volume production through Multi Project Wafer - MPW - and dedicated wafer runs.

EUROPRACTICE IC Service offers you a total solution for your ASIC development including :

- [ASIC Front-end Design through the EUROPRACTICE Alliance Network or Foundry Partners](#)
- [Deep Submicron RTL-to-layout Service](#)
- [ASIC Prototyping \(MPW runs\)](#)
- [ASIC low volume and ramp-up volume to high volume production delivering tested and qualified components](#)
- [Mems Prototyping \(MPW runs\)](#)
- [Silicon Photonics Prototyping\(MPW runs\)](#)
- [Design Contest](#)

For the European universities and research institutes, EUROPRACTICE offers special educational conditions through a contract with the European Commission in the frame FP6 and FP7 including :

- [Access to low cost CAD tools](#)
- [Special discounted prototype fabrication prices](#)

Latest news

[Annual Report 2010](#)

[imec-ePIXfab SiPhotonics MPW available now!](#)

[2011 TSMC Europractice Innovation Award](#)

[Wall Calendar 2011](#)

[Runschedule 2011](#)

[Winner UMC 90nm Design Contest -August 2010](#)

[TSMC 40nm available now!](#)

[More news](#)

Training

Contents:

- Technology
- Design rules
- Supply chain
- Procedures
- Hands-on design training



Next training: June 6-10, 2011, Grenoble, France

ePIXfab

- For R&D by universities, research institutes and companies world-wide
- Only already developed technologies

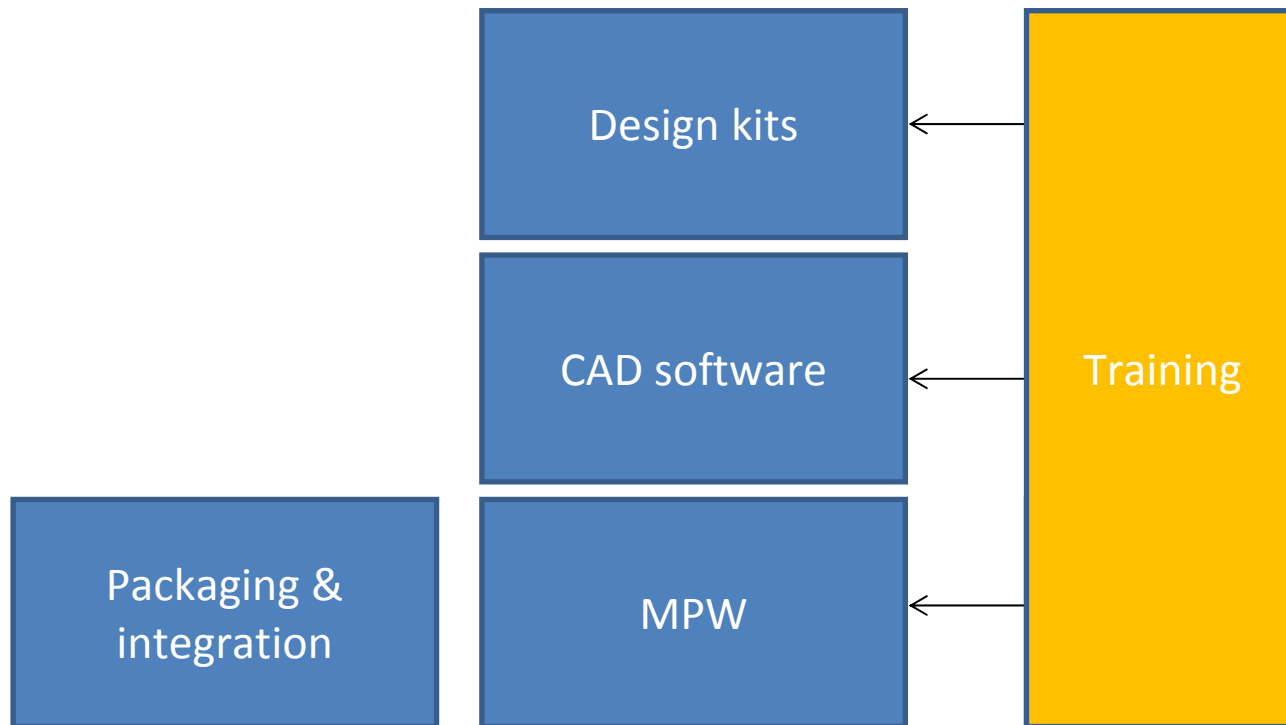
Some facts (since 2006)

- 13 MPW shuttles, 60 different users, 168 designs
- 43 universities, 12 research institutes, 4 SMEs, 1 larger company
- 35 Europe, 13 N-America, 10 Asia, 2 Australia, 1 Middle-East
- 3 training events, 3 workshops
- >650 website visitors, >10000 website visits

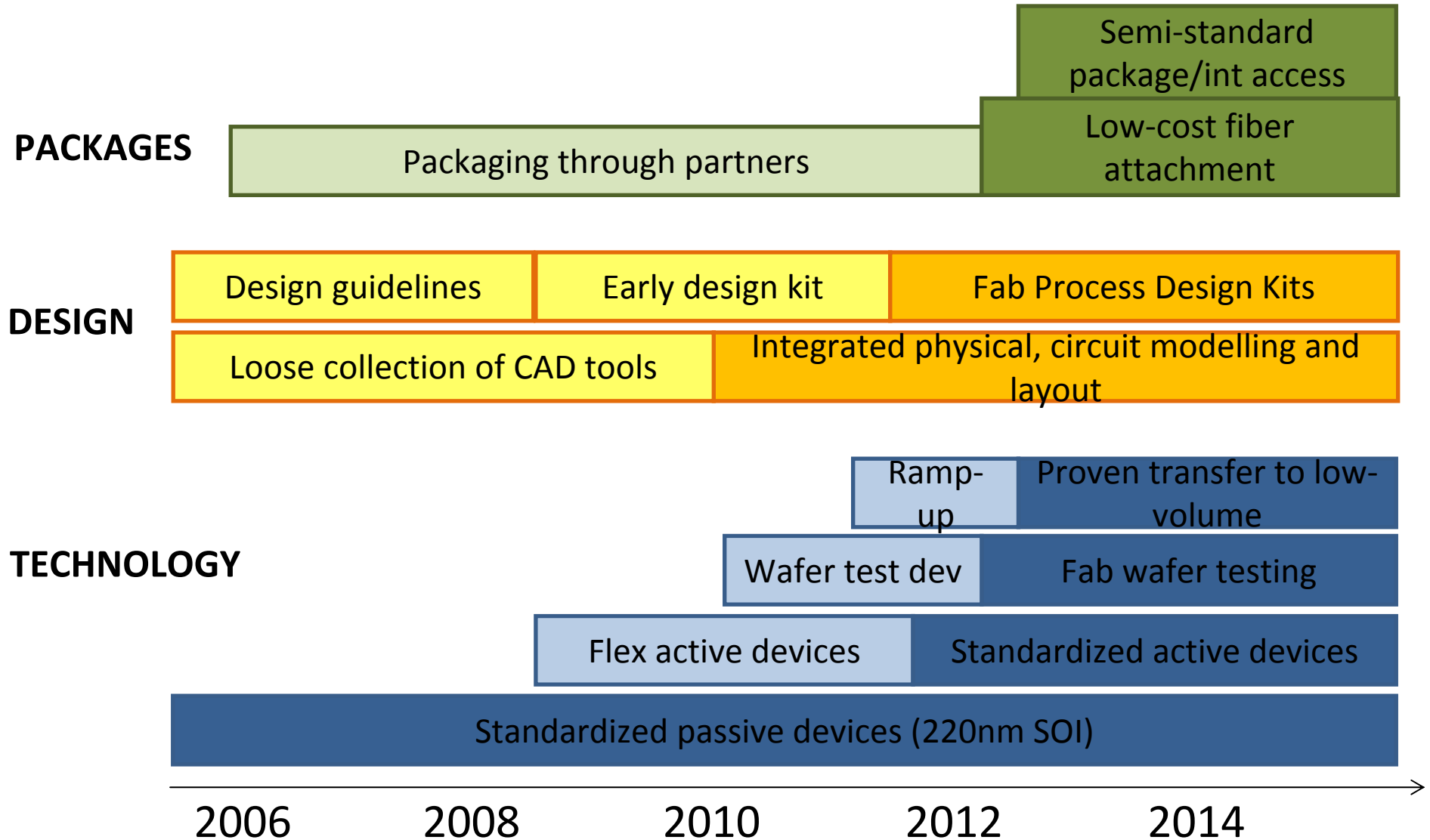
What's up next?

- Maturity of design flow and technology
- Standardized active/passive integration
- Access to packaging & integration services
- Focus on SMEs
- Single point of access to a larger consortium of Si photonics expertise centers

Service



Technology



Packaging

1. Low-cost fiber attachment and wirebonding
 - Test chips in a testbed/lab
 - ~10-20 chips
 - Not manufacturable, just for chip testing
2. Semi-standardized package approaches
 - Use chips in demonstrators and prototypes
 - Few chips
 - Path to manufacturing
 - Access to packaging, integration, testing expertise

Testing

- (Semi-)automated wafer testing being deployed at fabs (CEA-LETI, Imec)
- Some agreement on process & device benchmarks and test procedures needed (e.g.: waveguide performance, modulator performance, ...)

THANK YOU

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